
New Current Sensing Scheme for Static Transfer Switches



Solidstate Controls Incorporated
875 Dearborn Drive
Columbus, Ohio 43085
Tel : (614) 846-7500
Fax: (614) 885-3990

New Current Sensing Scheme for Static Transfer Switches

Abstract

This paper describes a simple overcurrent sensing circuit capable of recognizing high crest factor currents without time averaging. First, the static transfer switch itself is described. Then the new overcurrent sensing circuit, capable of practically measuring rms current levels with crest factors less than or equal to three is described. Finally, theoretical maximums and minimums are compared to measured results.

Introduction

Switching power supplies have been in use for at least 10 years. In 1981, 291/6 of the total U.S. market for power supplies was switching regulators. By 1985, 50% of the market is expected to be switching power supplies. (1)

One major disadvantage of switching power supplies is that they draw non-linear current waveforms exhibiting high crest factors or high relative peak currents. Other problems such as high harmonic currents, excessive currents in neutral conductors and common mode noise are also encountered when using switching power supplies. These have been previously discussed (2), and will not be detailed further here. Computer power supply designers are now preparing the next generation of supplies with one of the main objectives being elimination of non-linear, high crest factor current waveform. (3). Until the next generations of DC power supplies are commercially available and economical, the problems incurred by switching power supplies must be dealt with. Since ferroresonant inverters are particularly well suited for powering non-linear or high crest factor loads, the only challenge was to develop a static switch current sense capable of recognizing high crest factor currents.

The Static Switch

The purpose of a static switch in an uninterruptible power s*6m is to provide power to the load under all conditions. During normal operation the inverter is connected to the load through the static switch. However, during abnormal modes the static switch will transfer the load from the inverter (or preferred source) to the bypass (or some alternate) source of power. This configuration is referred to as a single UPS with bypass and transfer switch and is shown in **Figure 1**. In UPS employing ferroresonant inverters the static switch will transfer the load from inverter under the following conditions: 1) failure or deterioration of the inverter square wave; 2) failure or deterioration of the sinusoidal output voltage of the ferroresonant filter; or 3) branch load fault or simple overload which exceeds the current capacity of the inverter/CVT. A block diagram of the static switch is shown in **Figure 2**.

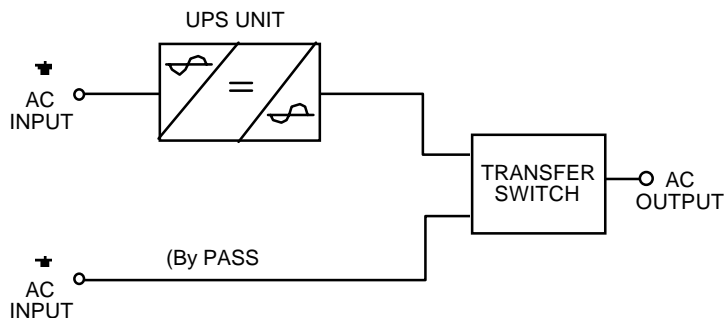


Figure 1 Single UPS with Bypass Transfer Switch *The AC inputs shall be from either a common source or separate sources.

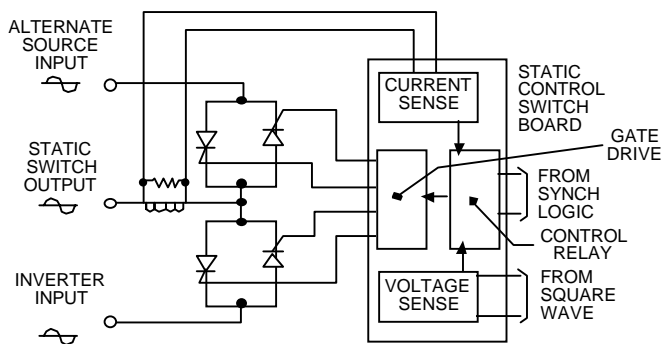


Figure 2 Static Switch Block Diagram

Current Sensing

The most important function of the current sense on the static switch control board is to transfer the load from the inverter to the bypass source in the event of a branch fault. When a fault occurs, it is imperative that the static switch transfer occurs instantaneously. Therefore it is undesirable to perform any time averaging on the value of the current waveform before initiation of transfer. For this reason the current sense circuit has been a peak detector. A simplified current sense schematic is shown in **Figure 3**. Q1 actually initiates the transfer by crowbaring a control relay. The problem in using this circuit for sending currents exhibiting high crest factor is that the static switch will transfer at a reduced percent of load. For example, if the static switch was calibrated to transfer on a linear sinusoidal current waveform at 120% of nominal output current, the static switch would transfer at 56% of load if current waveform exhibited a crest factor of 3. **Figure 4** shows an actual computer current waveform exhibiting a crest factor of 1.9. We can see the mixture of linear and non-linear waveforms. **Figure 5** is a photograph of a synthesized high crest factor current waveform. This waveform was generated by constructing a full wave rectified, capacitive load. This waveform exhibits a crest factor of 2.4 and was used in testing the new current sense circuit.

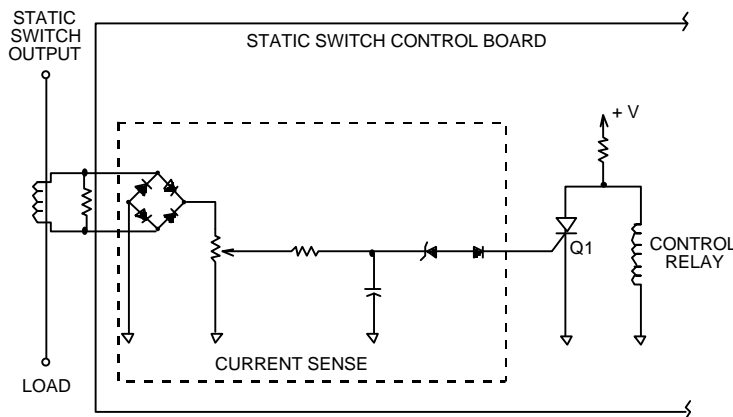


Figure 3 Peak Current Sense Unit

The new current sense circuit had to perform two functions: 1) provide instantaneous transfer of load to the bypass source in the event of a branch fault; and 2) transfer the load from the inverter to the bypass source if a true steady state overload condition exists. Another constraint immediately eliminated any true rms measurement of the output current. It was determined that a dual sensing scheme could be used if a device could be located with multiple inputs. Literature and product data was reviewed and a Motorola MC3423 (4) overvoltage "crowbar" sensing circuit was selected. The MX3423 is a mature device with multiple inputs and appropriate SCR gate drive output. The proposed circuit is presented in **Figure 6**. Circuit action is as follows: the static switch output current is transformed to a current of 1 ampere, converted to a voltage, full wave rectified and resistively divided to a usable voltage level. During a given half cycle, if the full wave rectified voltage exceeds a certain level, a constant current is fed into CT essentially starting a timer. If the full

wave rectified waveform remains above the reselected level for a time of approximately 2 milliseconds, a second internal level is exceeded and a transfer of load to the bypass source is initiated by Q 1 which is gated on. If during the timing interval the input waveform falls below the reference, an internal shunt transistor discharges CT at approximately ten times the charge rate and resets the timer. This circuit action performs the transfer when a steady state overload condition exists. By starting a 2 millisecond timer on a steady state overload, this portion of the circuit ignores the peak value of the current waveform. Two milliseconds were selected as the timing intervals for two reasons: 1) 2 milliseconds are quite typically the duration of a peak current due to switching power supplies; and 2) 2 milliseconds allow adequate time for completion of transfer in 1/4 cycle. A second detector, which is peak sensing, is calibrated to initiate a transfer if the peak corresponds to a crest factor of 3 or greater at I W16 load. The peak level detector initiates a transfer within 1 microsecond of detection. This is the mode of transfer when a fault condition exists.

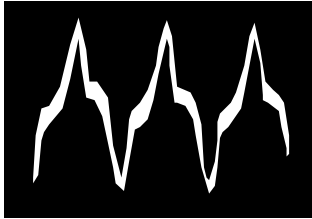


Figure 4 Actual computer load current waveform. Crest Factor ~ 1.9

Figure 7 illustrates basic circuit action. The top trace is the full wave rectified input waveform, and is present at pin 2 of the MC3423. The vertical cursor marks the point at which the reference level is exceeded. The portion of the top trace above the horizontal cursor is the portion of the waveform that is ignored until the peak attains a level corresponding to a crest factor of three at 100% load current. The middle trace is the waveform present at CT. The cursor marks the point where CT begins charging. When the voltage on CT achieves the reference level, the device produces an output gate drive, which fires the crowbar SCR. The bottom trace is the output waveform as viewed at pin 8 of the MC3423.

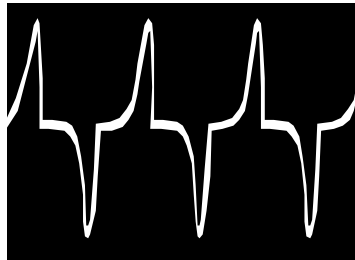


Figure 5 Synthesized Non-Linear current waveform. Crest Factor ~ 2.4

Test Results

Tests were performed to determine how well the new current sense circuit would respond to various crest factor levels. System output current was monitored with a rms responding Fluke multimeter with clamp-on.

Peak current levels were determined with an oscilloscope and shunt. To insure proper calibration, measurements were made with a purely linear load and crest factor was verified at 12. **Figure 8** demonstrates graphically the performance obtained. Results for the peak responding current sense vary closely paralleled calculated results. Results obtained from the new current sense circuit indicate that the rms transfer point actually increased slightly as the crest factor increased. Since the new current sense circuit is level detecting and not truly rms responding, it is not possible to predict exactly where transfer will occur with respect to crest factor and percent of load current. However, it is known that the static switch will not transfer below 120% of full load current, which is the desired transfer point, unless the crest factor of the load current exceeds three.

After laboratory tests were completed, a static switch with the new current sense circuit was installed in a field unit. Variable load and/or adjustable crest factors were not available. However, the computer load exhibited a crest factor of 2.2 at 120% of full load current. The static switch with the new current sense circuit was operated continuously for

6 months with no problems incurred. Transfers would occur only when load in excess of 120% were powered through the static switch.

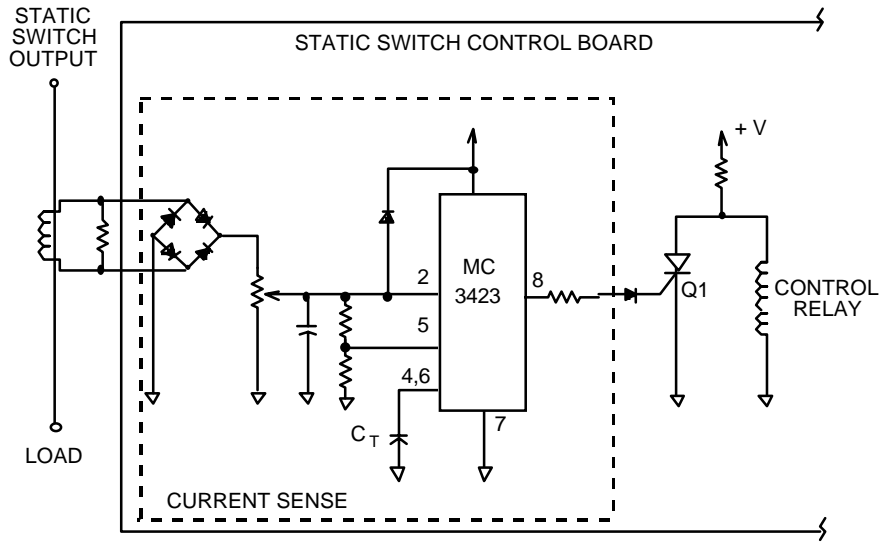
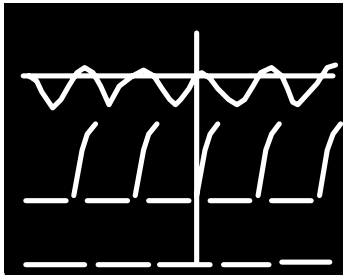


Figure 6 New Current Sense Circuit



TOP TRACE: Full Wave Rectified Input Waveform
 MIDDLE TRACE: Voltage On C_T
 BOTTOM TRACE: Output Gate Drive

Figure 7

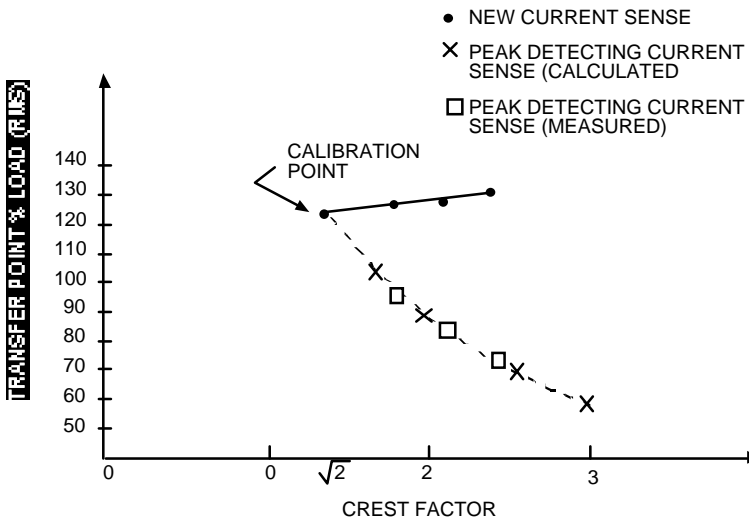


Figure 8 Transfer Point vs. Crest Factor

Conclusion

Switching power supplies draw non-linear high crest factor current waveforms. A simple current sensing circuit that provides instantaneous transfer yet is capable of recognizing high crest factors has been presented. The new current sense circuit has been implemented with a minimum device count, and uses simple mature devices, enhancing reliability. Tests have been performed and results have been presented, including field installation experience.

References

1. Arnold, William, "Power Supply Market Switches on to Switches," Electronic Business, June 1982, Pages 72-74.
2. Roberts, Bradford, "New Design Parameters for Computer Power Distribution," 4-7. Proceedings of Intelc 79. Washington D.C., November 26-29. 1979.
3. Aldridge, Tom, "A New Method for Reducing Line Current Crest Factor Due To Capacitive Input Filters," E-2 Proceedings of Powercon 9. Washington D.C.. July 13-15, 19B2.
4. "Motorola Linear Integrated Circuits," Series C, 1979, Motorola, Inc., Pages 6-125 to 6-130.